

## **FUJI POWER MOSFET**

# Super J MOS<sup>®</sup> S1 series

# N-Channel enhancement mode power MOSFET

# Features

Outline Drawings [mm]

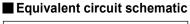
Low switching loss easy to use (more controllabe switching dV/dt by R<sub>g</sub>)

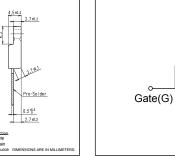
# Applications

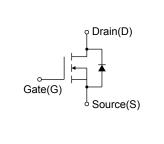
UPS Server Telecom Power conditioner system Power supply

Low on-state resistance

#### TO-220F(SLS) 2.7±0.2 £ 12 Pre-Solder 0.5 8.3 07±0.2 2.54±0.2 2.7 10.2 2.54 #0.2 123 Gate Drain -----







# Absolute Maximum Ratings at Tc=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V <sub>DS</sub>	600	V	
Dialit-Source voltage	VDSX	600	V	V <sub>GS</sub> =-30V
Continuous Drain Current	lo Rate	AD #22	A	Tc=25°C Note*1
Continuous Drain Current		日的一日日日日	А	Tc=100°C Note*1
Pulsed Drain Current	lop/	\$158 ±66 LA P	A	Note*1
Gate-Source Voltage	VGs ATT P	5 × (±30)	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	TAR	dreet	A	Note *2
Non-Repetitive Maximum Avalanche Energy	FANCE PI	548.9 548.9	J∘ mJ	Note *3
Maximum Drain-Source dV/dt	dVos/dt	5願し、50	kV/µs	V <sub>DS</sub> ≤ 600V
Peak Diode Recovery dV/dt	dv/dt tab a	igning80	kV/µs	Note *4
Peak Diode Recovery - di/dt	di/dt new ac-	100	A/µs	Note *5
Maximum Bower Discingtion tri目設計してなけ	entor ne	2.16	w	Ta=25°C
Maximum Power Dissipation 注:新規設計にはない。 Operating and Storage Temperature Pange		70	v	Tc=25°C
Operating and Storage Temperatury Ofe. Dor	Tch	150	°C	
Operating and Storage remperature range	Tstg	-55 to +150	°C	

 Note \*1 : Limited by maximum channel temperature.

 Note \*2 : Tch≤150°C, See Fig.1 and Fig.2

 Note \*3 : Starting Tch=25°C, IAs=4A, L=62.9mH, VDD=60V, RG=50Ω, See Fig.1 and Fig.2

 EAS limited by maximum channel temperature and avalanche current.

 Note \*4 : Ir≤-Io, -di/dt=100A/µs, VDS peak≤600V, Tch≤150°C.

 Note \*5 : Ir≤-ID, dV/dt=30kV/µs, VDS peak≤600V, Tch≤150°C.

#### Electrical Characteristics at Tc=25°C (unless otherwise specified) Static Ratings

Description	Symbol	Conditions		min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA V <sub>GS</sub> =0V		600	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	I₀=500µA V₀s=V₀s		3.0	4.0	5.0	V
Zero Gate Voltage Drain Current		V <sub>DS</sub> =600V V <sub>GS</sub> =0V	T <sub>ch</sub> =25°C	-	-	25	-μA
	IDSS	V <sub>DS</sub> =480V V <sub>GS</sub> =0V	T <sub>ch</sub> =125°C	-	120	-	
Gate-Source Leakage Current	lgss	V <sub>GS</sub> = ± 30V V <sub>DS</sub> =0V		-	10	100	nA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	I <sub>D</sub> =11A V <sub>GS</sub> =10V		-	0.144	0.170	Ω
Gate resistance	Rg	f=1MHz, open drain		-	3.5	-	Ω

#### Dynamic Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	g <sub>fs</sub>	I <sub>D</sub> =11A V <sub>DS</sub> =25V	9.5	19	-	S
Input Capacitance	Ciss	V <sub>DS</sub> =400V V <sub>GS</sub> =0V	-	1580	-	
Output Capacitance	Coss		-	47	-	
Reverse Transfer Capacitance	Crss	f=250kHz	-	3.5	-	
Effective output capacitance, energy related (Note *6)	C <sub>o(er)</sub>	V <sub>GS</sub> =0V V <sub>DS</sub> =0400V	-	125	-	pF
Effective output capacitance, time related (Note *7)	C <sub>o(tr)</sub>	V <sub>GS</sub> =0V V <sub>DS</sub> =0400V ID=constant	-	415	-	
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> =400V, V <sub>GS</sub> =10V I <sub>D</sub> =11A, R <sub>G</sub> =27Ω See Fig.3 and Fig.4	-	85	-	- ns
Turn-On Time	tr		-	27	-	
td(off)	td(off)		-	150	-	
Turn-Off Time	tr		-	18	-	
Total Gate Charge	QG		-	- 58 -	-	nC
Gate-Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> =400V, I <sub>D</sub> =22A	-	17.5	-	
Gate-Drain Charge	QGD	─ V <sub>GS</sub> =10V _ See Fig.5	-	23.5	-	
Drain-Source crossover Charge	Qsw		-	9	-	

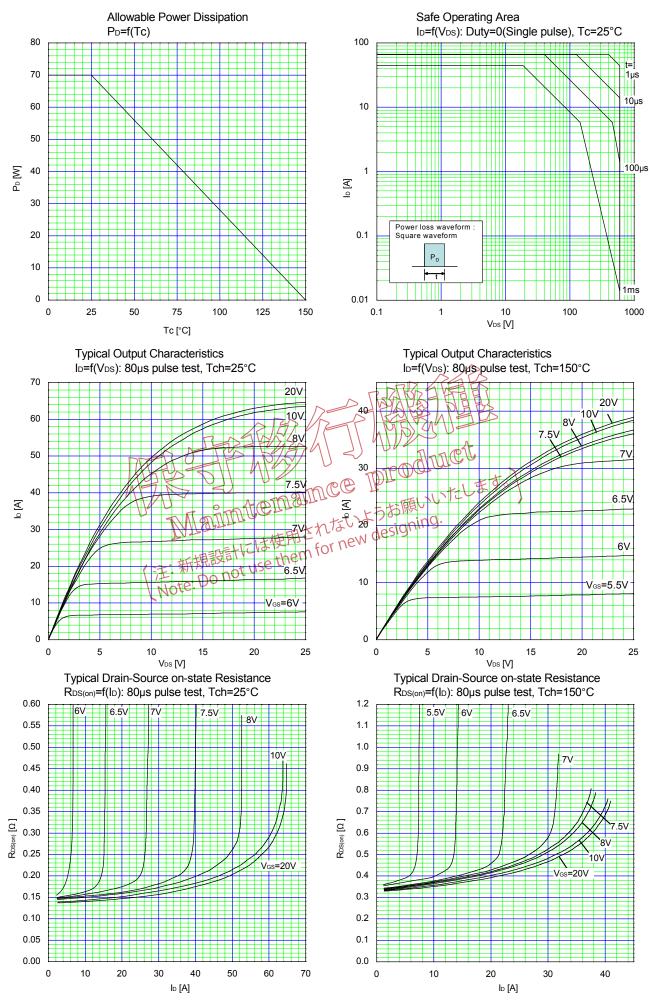
Note \*6 :  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V. Note \*7 :  $C_{o(tr)}$  is a fixed capacitance that gives the same charging times as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V.

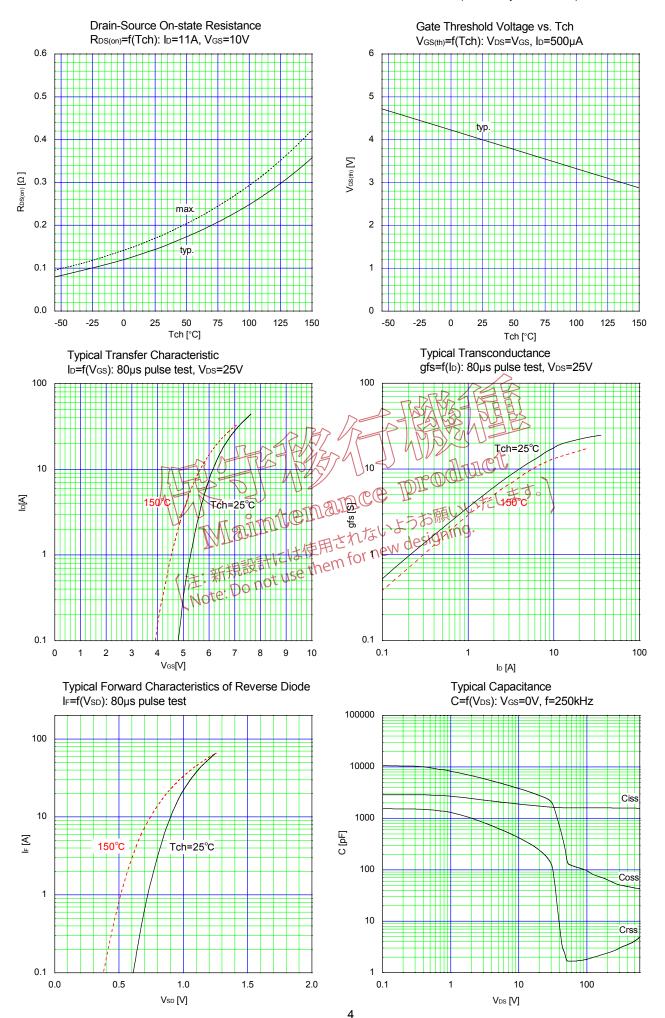
## Reverse Diode

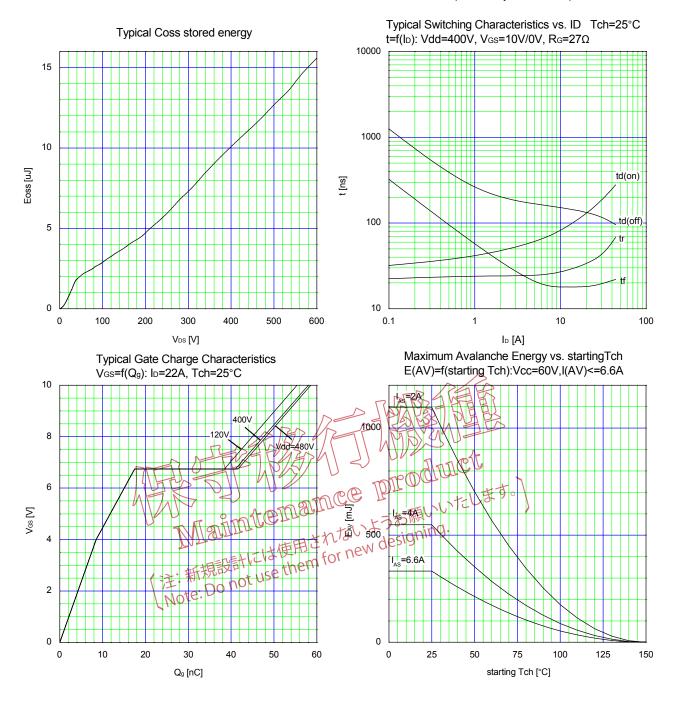
Description	Symbol	Conditions	min. typ.	max.	Unit
Avalanche Capability	lav R	L=14mH,T,=25°C See Fig.1 and/Fig.2	6.6 -	-	A
Diode Forward On-Voltage	Trap D	II=22AWds=0V Ten=25°C	TUICO #J.)	1.35	v
Reverse Recovery Time	to to	TER ALANCE TOOL	NTEL 165	-	ns
Reverse Recovery Charge	a MIai	The 25°C IN The 25°C INTERNATION OF THE 25°C INTERNATI	- 1.1	-	μC
Peak Reverse Recovery Current	泄.新規副	See Fig. 6 and Fig. 71 101	- 13.2	-	A

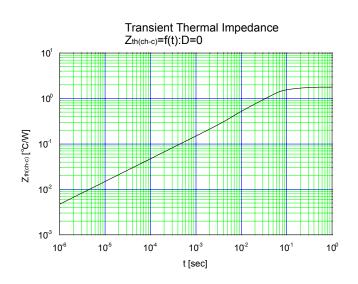
# Thermal Resistance

Parameter	Symbol	min.	typ.	max.	Unit
Channel to Case	Rth(ch-c)	-	-	1.79	°C/W
Channel to Ambient	Rth(ch-a)	-	-	58	°C/W









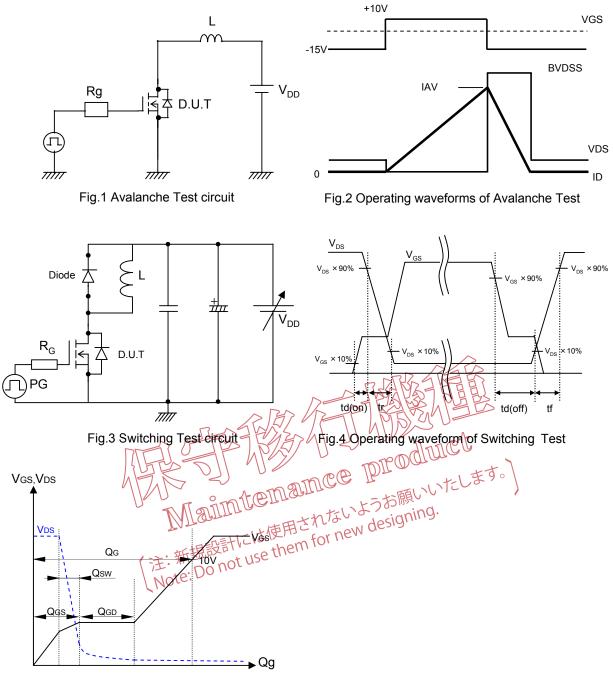


Fig.5 Operating waveform of Gate charge Test

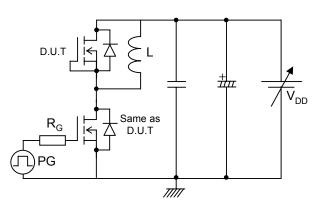


Fig.6 Reverse recovery Test circuit

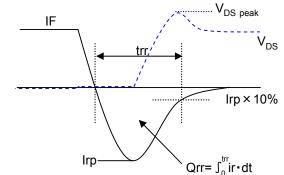
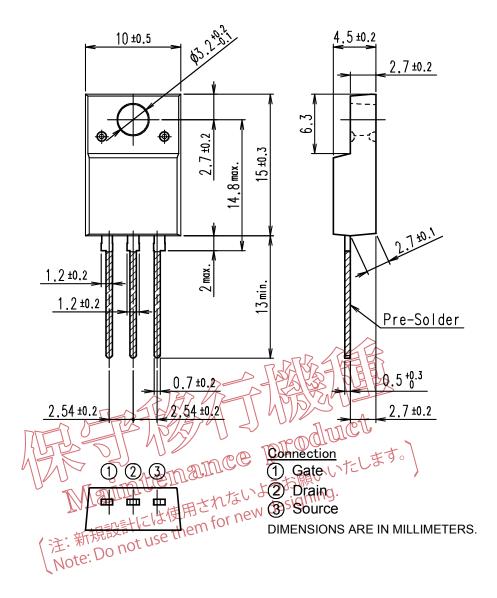
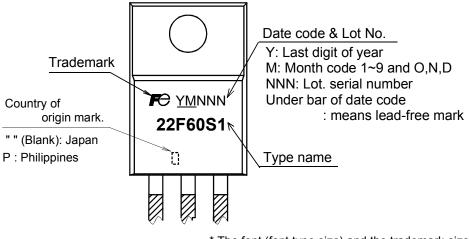


Fig.7 Operating waveform of Reverse recovery Test

# Outview: TO-220F(SLS) Package



# Marking



\* The font (font type,size) and the trademark-size might be actually different.

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