

# Innovating Energy Technology

http://www.fujielectric.com/products/semiconductor/ **FUJI POWER MOSFET** 

# Super J MOS<sup>®</sup> S1 series

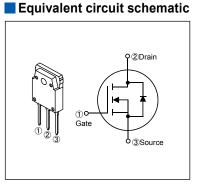
# N-Channel enhancement mode power MOSFET

## Features

Pb-free lead terminal **RoHS** compliant

Applications For switching

Outline Drawings [mm] TO-3P ф ф ф



# Absolute Maximum Ratings at Tc=25°C (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	VDS	600	V	
Dialit-Source voltage	VDSX	600	V	V <sub>GS</sub> =-30V
Continuous Drain Current	lo Rota	#20 A	А	Tc=25°C Note*1
Continuous Drain Current		172=126月目1	А	Tc=100°C Note*1
Pulsed Drain Current	IDP/	5 158 ±60 5 F	A	Note*1
Gate-Source Voltage	VGs CTC	5 × ±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	TAR	dract	A	Note *2
Non-Repetitive Maximum Avalanche Energy	Ence IPI	472.2 5	す∘ mJ	Note *3
Maximum Drain-Source dV/dt	dVos/dt	50、50	kV/µs	V <sub>DS</sub> ≤ 600V
Peak Diode Recovery dV/dt	dV/dt/500	igning 30	kV/µs	Note *4
Peak Diode Recovery - di/dt	di/dt new OF-	100	A/µs	Note *5
Maximum Davies Disainstian tr相設計化。the	m <sup>ror</sup> .	2.5	W	T₂=25°C
Maximum Power Dissipation	FD	140	vv	Tc=25°C
Operating and Storage Temperatury Operation	Tch	150	°C	
Operating and Storage reinperature range	T <sub>stg</sub>	-55 to +150	°C	

Note \*1 : Limited by maximum channel temperature. Note \*2 : Tch≤150°C, See Fig.1 and Fig.2 Note \*3 : Starting Tch=25°C, IAs=2A, L=216mH, Voo=60V, RG=50Ω, See Fig.1 and Fig.2

EAs limited by maximum channel temperature and avalanche current. Note \*4 : Ir≤-ID, -di/dt=100A/µs, VDs peak≤600V, Tch≤150°C.

Note \*5 : IF≤-ID, dV/dt=30kV/µs, VDS peak≤600V, Tch≤150°C.

#### Electrical Characteristics at T<sub>c</sub>=25°C (unless otherwise specified) Static Ratings

Parameter	Symbol	Conditions		min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I₀=250μA V₅s=0V		600	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	I₀=250µA V₀s=V₀s		3	4	5	V
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> =600V V <sub>GS</sub> =0V	T <sub>ch</sub> =25°C	-	-	25	- μA
		V <sub>DS</sub> =480V V <sub>GS</sub> =0V	T <sub>ch</sub> =125°C	-	100	-	
Gate-Source Leakage Current	IGSS	V <sub>GS</sub> = ± 30V V <sub>DS</sub> =0V		-	10	100	nA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	I <sub>D</sub> =10A V <sub>GS</sub> =10V		-	0.168	0.2	Ω
Gate resistance	Ro	f=1MHz, open drain		-	3.7	-	Ω

#### Dynamic Ratings

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	<b>g</b> <sub>fs</sub>	I <sub>D</sub> =10A V <sub>DS</sub> =25V	8	16	-	S
Input Capacitance	Ciss	V <sub>DS</sub> =400V	-	1370	-	
Output Capacitance	Coss	V <sub>GS</sub> =0V	-	40	-	
Reverse Transfer Capacitance	Crss	f=250kHz	-	3	-	
Effective output capacitance, energy related (Note *6)	Co(er)	V <sub>GS</sub> =0V V <sub>DS</sub> =0400V	-	115	-	pF
Effective output capacitance, time related (Note *7)	C <sub>o(tr)</sub>	V <sub>GS</sub> =0V V <sub>DS</sub> =0400V ID=constant	-	365	-	
Turn-On Time	t <sub>d(on)</sub>		-	80	-	
Turn-On Time	tr	$V_{DD}$ =400V, $V_{GS}$ =10V	-	27	-	- ns
Turn-Off Time	t <sub>d(off)</sub>	l₀=10A, R₀=27Ω _ See Fig.3 and Fig.4	-	124	-	
turn-Off Time	tr		-	19	-	
Total Gate Charge	QG		-	52	-	
Gate-Source Charge	Q <sub>GS</sub>	Vpp=400V, Ip=20A Vgs=10V See Fig.5	-	16	-	
Gate-Drain Charge	Q <sub>GD</sub>		-	20.5	-	nC
Drain-Source crossover Charge	Qsw		-	8.5	-	1

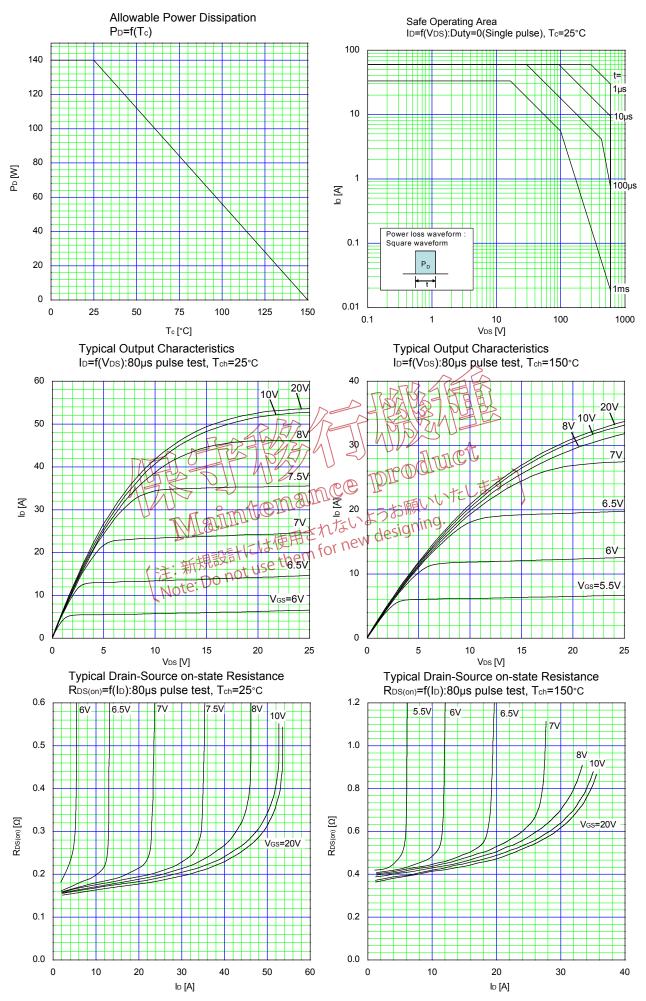
Note \*6 :  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V. Note \*7 :  $C_{o(tr)}$  is a fixed capacitance that gives the same charging times as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V.

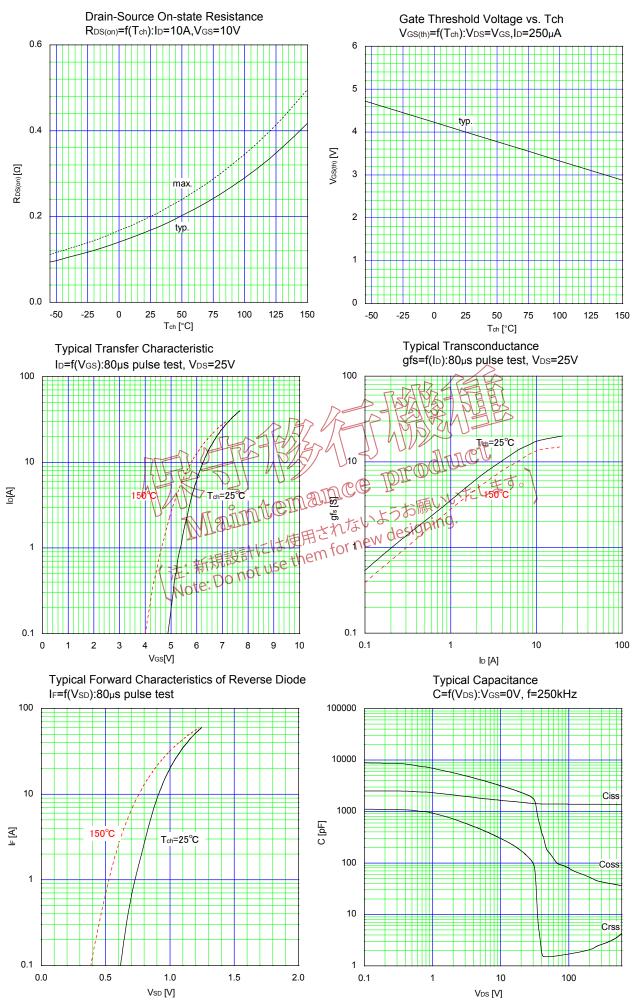
### Reverse Diode

Parameter	Symbol	Conditions	s min s	typ.	max.	Unit
Avalanche Capability	lav R	L=6.02mH, To=25°C See Fig. 7 and Fig. 2	6.6	-	-	А
Diode Forward On-Voltage	THE S	It=20A,Ves=0V Thn=25°C	TUICO	≠ <b>d</b> . \	1.35	V
Reverse Recovery Time	t	In=25℃ In=20A, Von=400V -di/dt=100A/ust thts To=725°€ (EAA) See Fig.6 and Fig.7 for new design not use	NUTEU	150	-	ns
Reverse Recovery Charge	Q. MIdi	-di/dt=100A/49日されない。 Tet=25(g使用されないのとのののののでのでのでのです。	-	1	-	μC
Peak Reverse Recovery Current 🎸	泄:新規副	not USE	-	13	-	А

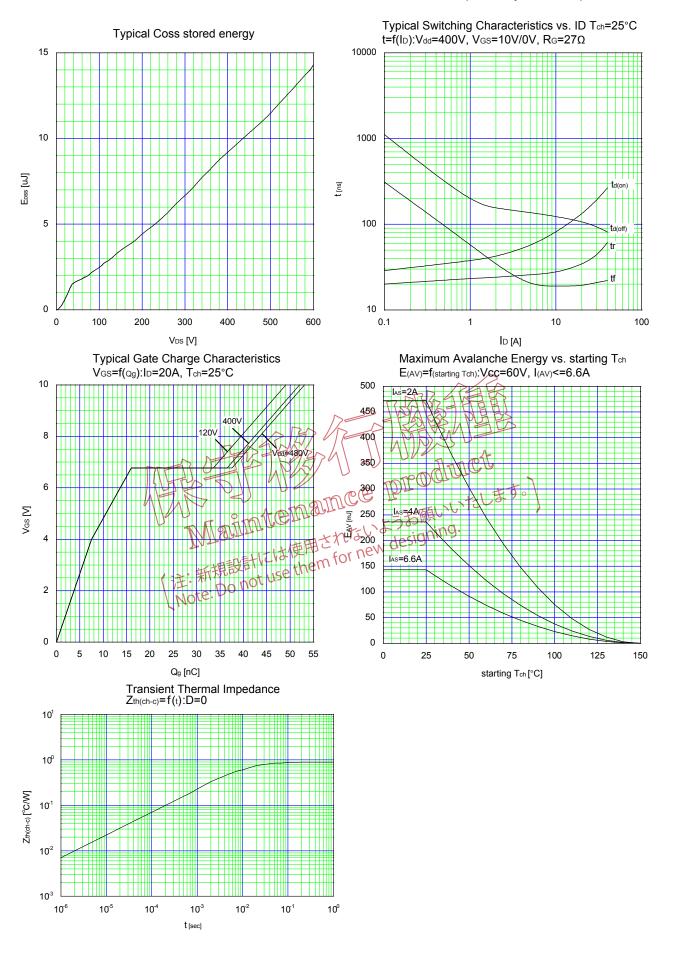
## Thermal Resistance

Parameter	Symbol	min.	typ.	max.	Unit
Channel to Case	R <sub>th(ch-c)</sub>	-	-	0.89	°C/W
Channel to Ambient	R <sub>th(ch-a)</sub>	-	-	50	°C/W





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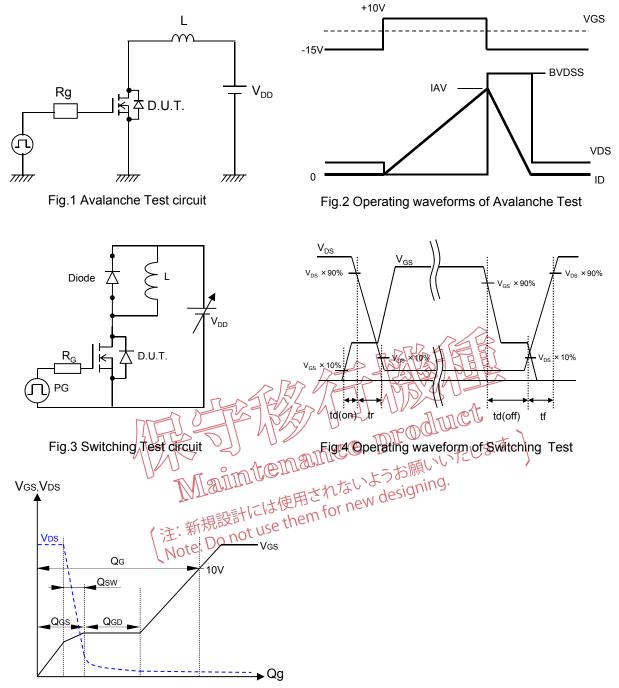
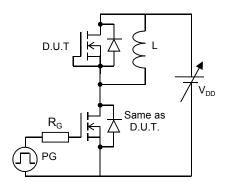


Fig.5 Operating waveform of Gate charge Test



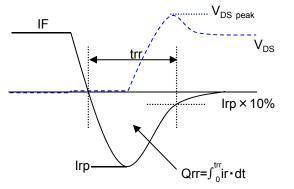
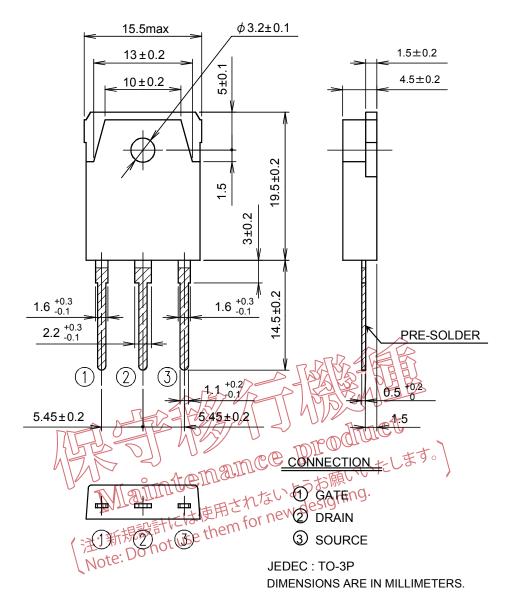


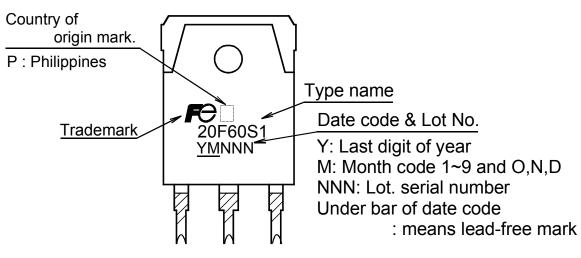
Fig.6 Reverse recovery Test circuit

Fig.7 Operating waveform of Reverse recovery Test

### Outview: TO-3P Package



#### Marking



\* The font (font type,size) and the trademark-size might be actually different.

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